REMARKS

Claims 1-9 are pending in this application. Claims 6-9 have been withdrawn from consideration as drawn to a non-elected invention.

Claims 1 and 2

The Office Action rejects claims 1 and 2 under 35 U.S.C. §103(a) over the combination of JP 10-275905 to Yamamoto (Yamamoto) and JP 10-335616 to Takada et al. (Takada). Applicants respectfully traverse this rejection.

Claim 1 is directed to a method for producing an SOI wafer by the hydrogen ion delamination, wherein after the delamination step, the wafer having an SOI layer is subjected to a two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing a rapid heating/rapid cooling apparatus and a batch processing type furnace.

The Office Action asserts that both RTA and batch processing type furnace are disclosed to be suitable for all portions of the annealing step, and suggests that employing RTA for the first portion and batch processing type furnace for the second portion of the annealing step, and that it would have been within the scope of one of ordinary skill in the art to employ either RTA or furnace annealing for almost the entire process and the other for a portion of the process that is insufficiently long to be expected to substantially alter the annealing step. However, one of ordinary skill in the art would not have been motivated to perform a two-type heat treatment, as alleged in the Office Action, without explicit motivation to combine a heat treatment by an RTA and a batch processing type furnace.

As described on page 8, lines 1-11 of the present specification, "if a wafer having an SOI layer is subjected to a heat treatment consisting of two stages utilizing separately a rapid heating/rapid cooling apparatus and batch processing type furnace after the delamination, surface crystallinity is restored and the surface roughness of short periods is improved in the heat treatment by the rapid heating/rapid cooling apparatus, and the surface roughness of long periods can be improved by the heat treatment utilizing the batch processing type furnace"

(emphasis added). For example, Tables 1 and 2 of the present specification compare Examples 1 and 2, in which a two-stage heat treatment utilizing the RTA apparatus and the batch processing type furnace was performed, and Comparative Example 1, in which a heat treatment utilizing only the RTA apparatus was performed, as to the surface roughness of 1 μm square (short periods). Although the values for Examples 1 and 2 and Comparative Example 1, before the heat treatment, were 7.21 - 7.45 nm, these values after the heat treatment were all within a range of 0.18 - 0.21 nm. That is, the surface roughness of short periods are improved sufficiently by RTA.

As to the surface roughness of 10 μm square (long periods), the values before the heat treatment were 5.50 - 5.80 nm. Although the values after the heat treatment on Examples 1 and 2 were sufficiently improved up to 0.28 - 0.38 nm, the values after the heat treatment on Comparative Example 1 were 1.60 nm, i.e., were not sufficiently improved. Thus, according the claimed invention, the surface roughness of short periods is improved in the heat treatment by RTA, and the surface roughness of long periods can be sufficiently improved further by the heat treatment utilizing the batch processing type furnace.

Yamamoto, in contrast to claim 1, discloses that a wafer having an SOI layer after the delamination is subjected to a heat treatment by RTA in an atmosphere containing hydrogen. Yamamoto performs a heat treatment in hydrogen atmosphere, but does not teach or suggest utilizing both an RTA and a batch processing type furnace, as claimed.

Thus, Yamamoto alone does not disclose, teach or suggest the invention of claims 1 and 2. Similarly, Takada, alone or combined with Yamamoto, does not disclose, teach or suggest the invention of claims 1 and 2.

Takada discloses that a wafer having an SOI layer after the delamination is subjected to a heat treatment of 1×10^{-6} to 1×10^{-11} Torr for 30-120 minutes. Takada inherently performs a heat treatment in the vacuum, which is different from the invention of claims 1 and 2, which perform a heat treatment in an atmosphere containing hydrogen or argon.

Further, Takada describes the average of surface roughness (Ra) for 10 μm square and 1 μm square before and after the heat treatment. After delamination, although the average of surface roughness before the heat treatment was 6.26 nm for 10 μm square (long periods, and 5.11 nm of 2 μm (short periods), respectively, the Ra values were changed to 1.16 nm and 0.38 nm, respectively, after the heat treatment at 850°C in the vacuum of 1×10^{-8} Torr. That is, although the surface roughness of short periods is improved by Takada's heat treatment in the vacuum, the surface roughness of long periods is not sufficiently improved.

Therefore, Takada alone does not disclose, teach or suggest the invention of claims 1 and 2. The combination of Yamamoto and Takada also does not disclose, teach or suggest the invention of claims 1 and 2.

Finding efficiencies that are peculiar to each heat treatment, and discussing that these efficiencies can be retained when the different heat treatments are combined, can be a motivation to combine a heat treatment by an RTA apparatus and that by a batch processing type furnace into a single process. However, there is no such motivation in either of the cited references. Accordingly, there is no possibility that one of ordinary skill in the art would have been motivated to perform a two-stage heat treatment by utilizing two different types of heat treatment apparatus, as in the claimed invention.

Takada's heat treatment essentially requires to be performed in the vacuum. Even if one of ordinary skill were to combine Yamamoto's heat treatment and Takada's heat treatment, the resulting combination would not result in performing a two-stage heat treatment in an atmosphere containing hydrogen or argon as in claims 1 and 2.

Furthermore, in response to Applicants' argument presented in the December 4, 2002, Request for Reconsideration, the Office Action points out that the present application's claims are not commensurate in scope with the process described as having unexpected results because the claims do not require any particular proportion of the annealing step to be

accomplished by either RTA or furnace annealing. Applicants disagree, at least because there is no requirement that such particular proportions be included in the claims.

However, none of the references disclose, teach or suggest that an SOI wafer having an SOI layer is subjected to a two-stage heat treatment by the rapid heating/rapid cooling apparatus after the delamination step, in the atmosphere containing hydrogen or argon. Therefore, claim 1 is distinguished from the cited art. One of ordinary skill in the art would understand from the present disclosure that each heat treatment temperature and time (proportion) of RTA and a batch processing type furnace could be optimized for the specific process. That is, without setting the proportion, claims 1 and 2 are distinguishable from the cited art, and further, the surface roughness can be improved in both long and short periods by two-stage heat treatment using two different apparatuses, rather than one stage heat treatment as separately disclosed in each of the cited references.

In addition, neither Yamamoto nor Takada contain motivation to combine RTA and a batch processing type furnace; thus, claim 1 cannot be derived from these references. Even if Yamamoto's heat treatment and Takada's heat treatment are combined, the combination cannot lead to claim 1 of this application, in which the two-stage heat treatment is performed in the atmosphere containing hydrogen or argon because Takada requires performing a heat treatment in the vacuum. Claim 1 also requires that an SOI wafer having an SOI layer is subjected to a two-stage heat treatment in an atmosphere containing hydrogen or argon utilizing a rapid heating/rapid cooling apparatus and a batch processing type furnace, which is clearly different from utilizing either apparatus separately, as is disclosed in the cited references.

For at least these reasons, Yamamoto and Takada, alone or in combination, do not teach or suggest the invention of claims 1 and 2. Accordingly, reconsideration and withdrawal of this rejection are requested.

Claims 3-5

The Office Action rejects claims 3-5 under 35 U.S.C. §103(a) over the combination of Yamamoto and Takada, and further in view of U.S. Patent No. 6,074,479 to Adachi et al. (hereinafter "Adachi") and Wolf et al., Vol. 1 (hereinafter "Wolf"). Applicants respectfully traverse this rejection.

Claim 3 is drawn to a method for producing an SOI wafer by the hydrogen ion delamination method, an FZ wafer, an epitaxial wafer or a CZ wafer of which COPs at least on the surface are reduced is used as the bond wafer, and the wafer having an SOI layer is subjected to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step. Claim 4 is drawn to a method for producing an SOI wafer, a CZ wafer produced from a single crystal ingot of which COPs are reduced for the whole crystal is used as the bond wafer. Claim 5 further limits claim 4 to the method in which the wafer having an SOI layer is subjected to a heat treatment under an atmosphere containing hydrogen or argon in a batch processing type furnace after the delamination step.

The Office Action applies Yamamoto and Takada to claims 3-5 in the same way the references were applied to claims 1 and 2, discussed in detail above. Yamamoto and Takada, alone or in combination, do not disclose, teach or suggest the invention of claims 3-5. The deficiencies of Yamamoto and Takada are not remedied by the secondary references of Adachi and Wolf.

Adachi discloses that wafers stacked up as shown in Fig. 1b are annealed in a furnace so that grown-in defects, which give rise to surface COP and internal COP, are eliminated. See Adachi, col. 1, lines 25-33. Wolf merely discloses that a CZ wafer can be obtained by processing such as slicing a single crystal ingot.

However, there is a problem that the buried oxide layer is etched through COPs in the SOI layer during the hydrogen annealing treatment to form pits if an SOI wafer is produced

by using a usual CZ wafer as the bond wafer. See, for example, Specification, page 4, line 12-page 5, line 7; page 6, line 24 - page 7, line 3. But, Applicants discovered that if a wafer without COPs or whose COPs are reduced is used as a bond wafer, as in claims 3-5, the COPs in SOI layer can be reduced or substantially eliminated, etching of the buried oxide layer due to COPs is not caused, and a heat treatment at a high temperature for a long period of time in a batch processing type furnace becomes possible. See Specification, page 10, lines 3-12, and page 11, lines 12-18.

Specifically, SOI wafers are produced by using as a bond wafer a CZ wafer produced from a single crystal ingot of which grown-in defects, such as COPs, are reduced for the whole crystal by controlling V/G (V: pulling rate, G: temperature gradient along the direction of solid-liquid interface of crystal) (see, for example, Example 3), or an epitaxial wafer (see, for example, Example 4), respectively, and then are subjected to a heat treatment utilizing a batch processing type furnace. See Specification page 40, line 27 - page 43; Table 3. Consequently, the surface roughness for both 1 μm square (short periods) and 10 μm square (long periods) are improved up to the same level as described above with reference to Examples 1 and 2. See Specification, Table 2. By producing an SOI wafer by using the wafer recited in claims 3 and 4 as a bond wafer, and after the delamination, performing a heat treatment in the atmosphere containing hydrogen or argon, generation of pits due to COPs can be prevented and a surface roughness for both short and long periods can be sufficiently improved.

In contrast, none of the cited references disclose, teach or suggest the existence of a problem that the buried oxide layer is etched through COPs in the SOI layer when the SOI wafer after the delamination is subjected to heat treatment in the atmosphere containing hydrogen or argon. Likewise, none of the cited references teach or suggest a solution to the problem, or motivation to combine these references to solve the unspecified problem. None of the references disclose, teach or suggest that generation of pits can be prevented, and none

of the references disclose, teach or suggest that a surface roughness for both short and long periods can be sufficiently improved by employing a bond wafer whose COPs in an SOI layer are reduced, and performing a heat treatment in the atmosphere containing hydrogen or argon. Therefore, one of ordinary skill in the art would not have been motivated to combine or modify these references to derive the inventions of claims 3-5, and the cited references, alone or in combination, do not disclose, teach or suggest the inventions of claims 3-5.

Thus, Yamamoto, Takada, Adachi and Wolf, alone or in combination, would not have rendered the invention of claims 3-5 obvious. Accordingly, reconsideration and withdrawal of this rejection is requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-9 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

William P. Berridge
Registration No. 30,024

Julie M. Seaman
Registration No. 51,156

WPB:JMS/jam

Date: June 12, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461